Basics of BJT bias design and some stability considerations

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J.L.

In this context a few practical examples are given to demonstrate strategies for designing reasonably stable biasing arrangements for bipolar transistors. The strategies involve initial configuration analysis calculations and typically a constraint equation, which enables to solve design equations based on the initial analysis. Some weak arguments for choosing the constraint equation are given using the results from stability factor calculations.

As a preliminary and shallow introduction, the stability factors need to be explained. For a BJT there exists three standard stability factors, which all relate to the temperature stability of either base-emitter voltage V_{BE}, the forward current gain factor β_F or the cut-off leakage current I_{CO}. The first two stability factors are simply defined as the partial derivatives

$$S(V_{BE}) = \frac{\partial I_C}{\partial V_{BE}} \qquad ; \qquad S(\beta_F) = \frac{\partial I_C}{\partial \beta_F}.$$

The leakage current related stability factor is kind of a special case, and without any detailed derivations, the common literature sometimes defines it as

$$S(I_{CO}) = \frac{1+\beta_F}{1-\beta_F\left(\dfrac{\partial I_B}{\partial I_C}\right)}.$$

Some of these factors will be somewhat carelessly used as an argument to justify the chosen constraint equations. Be warned not to trust the validity of the arguments too much. But all in all, it is clear that the biasing aims for stability against the variations in all of the above mentioned parameters. Most crucial is the large variation in β_F, but still that will not be analysed in this context because of the complexity of the resulting equations.

1 A BJT amplifier with voltage divider bias

The common-emitter amplifier with voltage divider resistors at the base and emitter resistor included offers the best possible stability of all BJT biasing schemes. Figure 1 indicates the components that affect the static currents and voltages in this common-emitter BJT amplifier. To make the analysis easier, the figure includes a clear nomenclature for all the currents and voltage nodes of the circuit.

Let's write a few analysis equations and see what are the key components that affect to the stability of this configuration. Since the stability criteria are analysed using currents, it is better to write the analysis equations as current

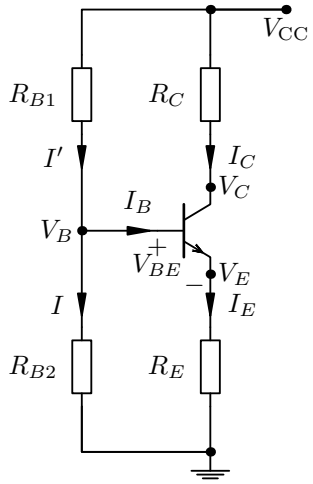

Figure 1: A DC model of the basic BJT amplifier with voltage divider bias

equations. For this bias model we need to cover only the base and emitter branches, because the collector branch is kind of independent from the base and emitter. There are two branches in the base and emitter circuit in Figure 1. The current equations for those branches are

$$V_{CC} = (I + I_B)R_{B1} + V_{BE} + (I_B + I_C)R_E$$
$$IR_{B2} = V_{BE} + (I_B + I_C)R_E.$$

Please note the relation $I' = I + I_B$, which has been used in the branch equations. The two branch equations can be combined into one analysis equation

$$V_{CC} = (I_B + I_C)R_E\left(1 + \frac{R_{B1}}{R_{B2}}\right) + I_B R_{B1} V_{BE}\left(1 + \frac{R_{B1}}{R_{B2}}\right). \tag{1}$$

For I_{CO} stability factor the derivative $\dfrac{\partial I_B}{\partial I_C}$ is needed. The previous equation can be differentiated in place with respect to I_C to yield

$$0 = \left(\frac{\partial I_B}{\partial I_C} + 1\right) R_E\left(1 + \frac{R_{B1}}{R_{B2}}\right) + \frac{\partial I_B}{\partial I_C} R_{B1},$$

from where

$$\frac{\partial I_B}{\partial I_C} = -\frac{R_E\left(1 + \dfrac{R_{B1}}{R_{B2}}\right)}{R_E\left(1 + \dfrac{R_{B1}}{R_{B2}}\right) + R_{B1}} = -\frac{R_E}{R_E + R_{B1}||R_{B2}},$$

where $R_{B1}||R_{B2}$ means the parallel resistance of the two resistors. Then we can use the stability equation for I_{CO}:

$$S(I_{CO}) = \frac{1 + \beta_F}{1 - \beta_F\left(\dfrac{\partial I_B}{\partial I_C}\right)} = \frac{1 + \beta_F}{1 + \beta_F\left(\dfrac{R_E}{R_E + R_{B1}||R_{B2}}\right)}.$$

The smaller the stability factor is, the better stability is obtained. Therefore, from here we can note that for good stability the resistance $R_{B1}||R_{B2}$ should be small compared to R_E. However, making $R_{B1}||R_{B2}$ small will decrease the input impedance and increase current consumption. So a rule must be invented to say when $R_{B1}||R_{B2}$ is small enough.

In the literature it is stated that the key pointer for bias stability for this configuration is to aim for

$$\frac{R_{B1}R_{B2}}{R_{B1}+R_{B2}} = \frac{1}{10}R_E(\beta_F+1). \tag{2}$$

This can be also interpreted as the rule of '1:10', where the idea is that currents which are a decade smaller can be assumed negligible in the analysis. The rule of 1:10 can be made also variable, so that

$$\frac{R_{B1}R_{B2}}{R_{B1}+R_{B2}} = \frac{1}{m}R_E(\beta_F+1). \tag{3}$$

From equation (1) we can derive an equation for the base current

$$I_B = \frac{V_{CC}\dfrac{R_{B2}}{R_{B1}+R_{B2}} - V_{BE}}{\dfrac{R_{B1}R_{B2}}{R_{B1}+R_{B2}} + R_E(\beta_F+1)},$$

from where

$$\frac{R_{B2}}{R_{B1}+R_{B2}} = \frac{\dfrac{I_C}{\beta_F}\left[\dfrac{R_{B1}R_{B2}}{R_{B1}+R_{B2}} + R_E(\beta_F+1)\right] + V_{BE}}{V_{CC}}. \tag{4}$$

After dividing equation (3) by (4)

$$R_{B1} = \frac{R_E(\beta_F+1)V_{CC}}{mV_{BE} + (m+1)R_E(\beta_F+1)\dfrac{I_C}{\beta_F}}, \tag{5}$$

where $m \geq 10$ is required for stable biasing. Furthermore, if R_C is known, the collector current is

$$I_C = \frac{V_{CC}-V_C}{R_C},$$

which enables to define R_{B1} according to the desired collector bias voltage V_C. Once R_{B1} is known, the other base resistor is evaluated from the equation

$$R_{B2} = \frac{R_E(\beta+1)}{m - \dfrac{R_E}{R_{B1}}(\beta+1)}. \tag{6}$$

To conclude, the bias design procedure could go as follows:

1. select the operating voltage V_{CC}
2. select the collector bias voltage V_C
3. select R_C to determine collector current, gain and output impedance
4. select R_E so that the emitter bias voltage V_E is close to V_{BE}
5. select the stability multiplier m, which should be larger or equal to 10
6. calculate R_{B1} from equation (5)
7. calculate R_{B2} from equation (6)

2 A BJT AMPLIFIER WITH COLLECTOR-TO-BASE BIAS

The simplest biasing arrangement using the least amount of components is the collector-to-base bias, which is shown in Figure 2.

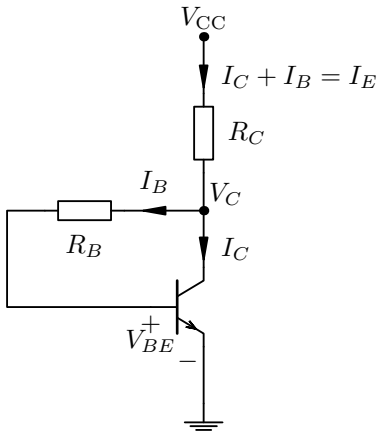

Figure 2: A basic collector-to-base bias arrangement

Because there is not that many design choices to be made in this configuration, it is easy to develop a relatively simple design model for biasing the circuit for a given collector voltage V_C. From Figure 2 one has

$$V_{CC} = V_{BE} + I_B R_B + (I_B + I_C) R_C = I_C \left(R_C + \frac{R_C}{\beta_F} + \frac{R_B}{\beta_F} \right) + V_{BE} \qquad (7)$$

and from here the quiescent collector current is

$$I_C = \frac{\beta_F (V_{CC} - V_{BE})}{R_B + R_C(\beta_F + 1)}. \qquad (8)$$

Let's assume that one wants to use a transistor with a certain β_F and collector resistor R_C. Then, from (7) and from (8) with selected collector voltage V_C one has

$$R_B = R_C(\beta_F + 1)\left[\frac{V_C - V_{BE}}{V_{CC} - V_C}\right]. \tag{9}$$

That is the only possible design equation to obtain the desired collector voltage V_C for this configuration. But let's address the stability of this bias method. The stability factor $S(I_{CO})$ needs the partial derivative

$$\frac{\partial I_B}{\partial I_C} = \frac{R_C}{R_C + R_B},$$

which is derived from equation (7). Already from here we see that for better stability R_B should be as small as possible compared to R_C. However, in this configuration that kind of design choice is seldom possible.

Let's see if the stability can be at least partially enhanced. Because the emitter is tied to ground, it can be assumed that the changes in V_{BE} are relatively critical for messing up the bias voltages. The stability factor $S(V_{BE})$ in this case is

$$S(V_{BE}) = \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta_F}{R_B + R_C(\beta_F + 1)}. \tag{10}$$

Then the next step is to analyse the same configuration with an emitter resistor added.

But for this specific configuration as a conclusion, the bias design procedure could go as follows:

1. select the operating voltage V_{CC}
2. select the collector bias voltage V_C
3. select R_C to determine collector current and output impedance
4. calculate R_B from equation (9)

3 A BJT AMPLIFIER COLLECTOR-TO-BASE BIAS WITH EMITTER RESISTOR

The circuit shown in Figure 3 is the same circuit as in the previous section, but now an emitter resistor is added to the configuration. Let's see what kind of effect does it have.

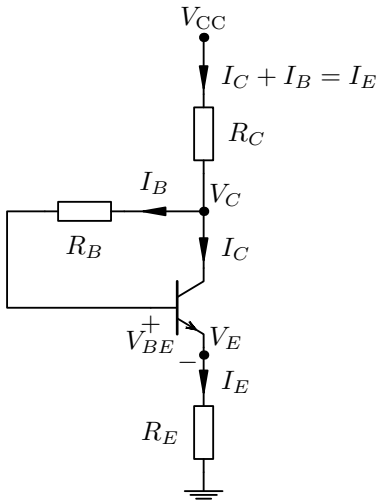

Figure 3: A collector-to-base bias arrangement with emitter resistor

Now, from Figure 3 one has

$$V_{CC} = V_{BE}+I_B R_B+(I_B+I_C)(R_C+R_E) = I_C\left(R_C + R_E + \frac{R_C+R_E}{\beta_F} + \frac{R_B}{\beta_F}\right)+V_{BE} \tag{11}$$

and from here the quiescent collector current is

$$I_C = \frac{\beta_F(V_{CC} - V_{BE})}{R_B + (R_C + R_E)(\beta_F + 1)}. \tag{12}$$

Let's assume that one wants to use a transistor with a certain β_F, a selected collector resistor R_C and a selected emitter resistor R_E. Then, from (11) and from (12) with a selected collector voltage V_C one has

$$R_B = \frac{(V_{CC} - V_{BE})R_C(\beta_F + 1) - (V_{CC} - V_C)(R_C + R_E)(\beta_F + 1)}{V_{CC} - V_C} \tag{13}$$

Next let's see how the stability factor $S(V_{BE})$ has changed. The stability factor $S(V_{BE})$ in this case is

$$S(V_{BE}) = \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta_F}{R_B + (R_C + R_E)(\beta_F + 1)}. \tag{14}$$

So as a conclusion, compared to equation (10) adding R_E slightly enhances the base-to-emitter voltage stability. One cannot choose to have R_E very large in this configuration, however. Also, when considering AC gain, it would be best to bypass the emitter resistor with a capacitor, then it would also be possible to use the standard feedback analysis to this circuit. Without a bypass capacitor, there exists two feedback paths (voltage and current feedback) from output to input. This combination of two feedback paths complicates the AC analysis considerably.

4 A BJT amplifier with enhanced collector-to-base bias

Still continuing with a collector-to-base feedback biasing, but now we try to make it better by introducing a second base bias resistor to the picture. The configuration is drawn to Figure 4 for clarity.

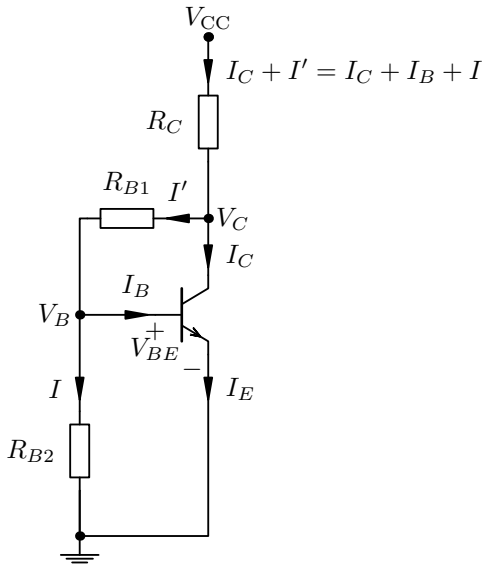

Figure 4: A collector-to-base bias arrangement with voltage divider at the base

Taking the same approach as earlier, the branch current equation is

$$V_{CC} = (I_B + I_C)R_C + \frac{V_{BE}}{R_{B2}}(R_C + R_{B1}) + I_B R_{B1} + V_{BE}. \tag{15}$$

After differentiation of equation (15), the partial derivative related to the stability factor $S(I_{CO})$ is

$$\frac{\partial I_B}{\partial I_C} = \frac{R_C}{R_C + R_{B1}}.$$

Since in this configuration the feedback resistor R_{B1} is typically smaller than in the simpler collector-to-base bias model, one can conclude that adding the other base resistor increases the bias stability.

Also, from equation (15) one can solve the collector current

$$I_C = \beta_F \frac{V_{CC} - \frac{V_{BE}}{R_{B2}}(R_{B1} + R_{B2} + R_C)}{R_{B1} + R_C(\beta_F + 1)}.$$

This leads to the V_{BE} stability factor

$$S(V_{BE}) = \frac{\partial I_C}{\partial V_{BE}} = -\frac{\frac{\beta_F}{R_{B2}}(R_{B1} + R_{B2} + R_C)}{R_{B1} + R_C(\beta_F + 1)}. \tag{16}$$

On its own this equation does not tell much about stability, but it is derived here to be compared later when an emitter resistor is included in the model.

For further analysis one can solve equation for the collector voltage V_C. This is done using the nodal analysis, where the current equation for the collector node is

$$I'_C = I_C + I' = \beta_F(I' - I) + I'.$$

The essential currents can be expressed with the node voltages as:

$$I'_C = \frac{V_{CC} - V_C}{R_C} \quad ; \quad I' = \frac{V_C - V_{BE}}{R_{B1}} \quad ; \quad I = \frac{V_{BE}}{R_{B2}}.$$

Substitutions of the voltage equations into the current equations leads to the equation

$$\frac{V_{CC} - V_C}{R_C} = (\beta_F + 1)\frac{V_C - V_{BE}}{R_{B1}} - \beta_F \frac{V_{BE}}{R_{B2}}.$$

From this equation one can solve the collector voltage, which is

$$V_C = \frac{V_{CC}R_{B1} + V_{BE}R_C\left(\beta_F \dfrac{R_{B1}}{R_{B2}} + \beta_F + 1\right)}{R_{B1} + (\beta_F + 1)R_C}. \tag{17}$$

The key for the design is to use R_{B2} to set the current in the base branch. This is obvious, since the voltage over R_{B2} is always V_{BE}. The same '1:10' rule which was used in the voltage divider bias configuration applies to this situation as well. A reasonable choice is

$$\frac{V_{BE}}{R_{B2}} \approx \frac{I_C}{10},$$

from where it follows that

$$R_{B2} \approx \frac{10V_{BE}R_C}{V_{CC} - V_C}, \tag{18}$$

if expressing it using the collector voltage V_C. In this case the factor 10 can be made a variable, but here it works upside down compared to the voltage divider bias plan. Larger values of the factor make R_{B2} larger and therefore suppress the current flowing in the base branch. For optimum stability, the current in the base branch should be as large as possible, but preferably not larger than I_C.

After the value for R_{B2} has been determined, then from equation (17)

$$R_{B1} = \frac{(V_C - V_{BE})(\beta_F + 1)R_C}{V_{CC} - V_C + \beta_F V_{BE}\dfrac{R_C}{R_{B2}}}. \tag{19}$$

To conclude, the bias design procedure for this configuration could go as follows:

1. select the operating voltage V_{CC}
2. select the collector bias voltage V_C
3. select R_C to determine collector current and output impedance
4. select the stability multiplier m, which should be approximately 10
5. calculate R_{B2} from equation (18)
6. calculate R_{B1} from equation (19)

5 A BJT AMPLIFIER ENHANCED COLLECTOR-TO-BASE BIAS WITH EMITTER RESISTOR

Trying the same trick as before to see what happens when an emitter resistor is added to the circuit. The configuration with added emitter resistor is drawn to Figure 5, which includes all the necessary currents and voltage nodes.

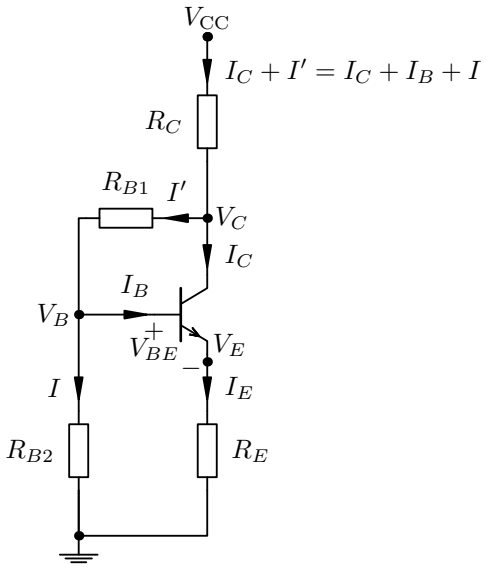

Figure 5: A collector-to-base bias arrangement with voltage divider at the base and emitter resistor

This configuration has two branch current equations:

$$V_{CC} = (I_B + I_C)R_C + I(R_C + R_{B1}) + I_B R_{B1} + V_{BE} + (I_B + I_C)R_E$$
$$IR_{B2} = V_{BE} + (I_B + I_C)R_E.$$

Combining these two equations we get

$$V_{CC} = \left(1 + \frac{R_E}{R_{B2}}\right)(I_B + I_C)R_C + \left(1 + \frac{R_E}{R_{B2}}\right) I_B R_{B1} + I_C R_E \frac{R_{B1}}{R_{B2}} + (I_B + I_C)R_E + \frac{V_{BE}}{R_{B2}}(R_{B1} + R_{B2} + R_C) \quad (20)$$

and the collector current can be solved from here,

$$I_C = \beta_F \frac{V_{CC} - \frac{V_{BE}}{R_{B2}}(R_{B1} + R_{B2} + R_C)}{\left(1 + \frac{R_E}{R_{B2}}\right)[R_{B1} + R_C(\beta_F + 1)] + R_E\left(\beta_F \frac{R_{B1}}{R_{B2}} + \beta_F + 1\right)}.$$

This leads to the V_{BE} stability factor

$$S(V_{BE}) = \frac{\partial I_C}{\partial V_{BE}} = -\frac{\frac{\beta_F}{R_{B2}}(R_{B1} + R_{B2} + R_C)}{\left(1 + \frac{R_E}{R_{B2}}\right)[R_{B1} + R_C(\beta_F + 1)] + R_E\left(\beta_F \frac{R_{B1}}{R_{B2}} + \beta_F + 1\right)},$$

so clearly adding R_E will lower the value of the stability factor when comparing to equation (16) and therefore increases the stability of the biasing configuration.

For further analysis one can solve equation for the collector voltage V_C. According to the Kirchhoff's current rule, the current equation for the voltage node V_B is:

$$I' = I + I_B = I + \frac{I_E}{\beta_F + 1}, \quad (21)$$

and for the voltage node V_C:

$$I'_C = I_C + I' = I_E \frac{\beta}{\beta_F + 1} + I'. \quad (22)$$

After the current equations are written down for each voltage node, the next step is to express the currents using the supply voltage and the node voltages. The currents appearing in the current equations can be expressed with respect to the node voltage as:

$$I'_C = \frac{V_{CC} - V_C}{R_C} \quad ; \quad I_E = \frac{V_B - V_{BE}}{R_E} \quad ; \quad I' = \frac{V_C - V_B}{R_{B1}} \quad ; \quad I = \frac{V_B}{R_{B2}}$$

and after substituting these voltage equations to the current equations,

$$\frac{V_{CC}-V_B}{R_C}=\frac{V_B-V_{BE}}{R_E}\frac{\beta}{\beta+1}+\frac{V_C-V_B}{R_{B1}}$$
$$\frac{V_C-V_B}{R_{B1}}=\frac{V_B}{R_{B2}}+\frac{V_B-V_{BE}}{R_E}\frac{1}{\beta+1}.$$

These two equations can be rearranged into a matrix equation from where the node voltages can be solved systematically:

$$\begin{bmatrix}\frac{\beta}{\beta+1}\frac{1}{R_C}+\frac{1}{R_{B1}} & \frac{\beta}{\beta+1}\frac{1}{R_E}-\frac{1}{R_{B1}}\\ -\frac{1}{R_{B1}} & \frac{1}{R_{B1}}+\frac{1}{R_{B2}}+\frac{1}{\beta+1}\frac{1}{R_E}\end{bmatrix}\times\begin{bmatrix}V_C\\ V_B\end{bmatrix}=\begin{bmatrix}\frac{V_{CC}}{R_C}+\frac{\beta}{\beta+1}\frac{V_{BE}}{R_E}\\ \frac{1}{\beta+1}\frac{V_{BE}}{R_E}\end{bmatrix}.$$

From the matrix equation one can calculate the analytic expression to verify the collector voltage with the chosen bias values:

$$V_C=\frac{V_{CC}[R_E(\beta_F+1)(R_{B1}+R_{B2})+R_{B1}R_{B2}]+V_{BE}R_C[R_{B2}(\beta_F+1)+\beta_F R_{B1}]}{\frac{\beta_F}{\beta_F+1}[R_E(\beta_F+1)(R_{B1}+R_{B2})+R_{B1}R_{B2}]+R_C(\beta_F+1)(R_E+R_{B2})}. \tag{23}$$

Because of the emitter resistor, the design equations change slightly. A reasonable, but approximate, choice for the design equation is

$$\frac{I_C R_E+V_{BE}}{R_{B2}}\approx\frac{I_C}{10},$$

from where it follows that

$$R_{B2}\approx 10\left(R_E+\frac{V_{BE}R_C}{V_{CC}-V_C}\right), \tag{24}$$

if expressing it using the collector voltage V_C.

After the value for R_{B2} has been determined, then from equation (23)

$$R_{B1}=\frac{R_C(\beta_F+1)[V_C(R_E+R_{B2})-V_{BE}R_{B2}]-\left(V_{CC}-\frac{\beta_F}{\beta_F+1}V_C\right)R_E(\beta_F+1)R_{B2}}{\left(V_{CC}-\frac{\beta_F}{\beta_F+1}V_C\right)[R_E(\beta_F+1)+R_{B2}]+V_{BE}R_C\beta_F}. \tag{25}$$

When considering AC gain, it would be best to bypass the emitter resistor with a capacitor, then it would also be possible to use the standard feedback analysis to this circuit. Without a bypass capacitor, there exists two feedback paths (voltage and current feedback) from output to input. This combination of two feedback paths complicates the AC analysis considerably.

To conclude, the bias design procedure for this configuration could go as follows:

1. select the operating voltage V_{CC}
2. select the collector bias voltage V_C
3. select R_C to determine collector current and output impedance
4. select R_E to increase bias stability, but don't use too big resistors
5. select the stability multiplier m, which should be approximately 10
6. calculate R_{B2} from equation (24)
7. calculate R_{B1} from equation (25)

6 The emitter follower

The basic BJT emitter follower is drawn in Figure 6.

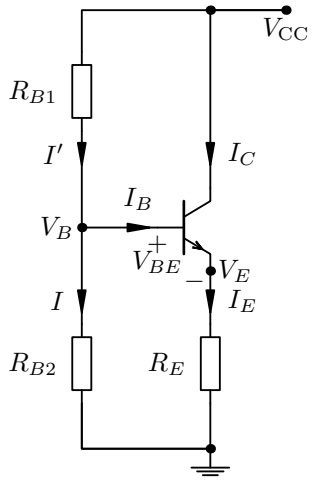

Figure 6: A BJT emitter follower

This configuration is not given a thorough walkthrough, because the analysis and design is awfully similar to the common emitter amplifier with voltage divider bias. The same design rule applies also here, namely

$$\frac{R_{B1}R_{B2}}{R_{B1}+R_{B2}} = \frac{1}{m}R_E(\beta_F+1), \tag{26}$$

where m should be approximately 10 or larger.

For this configuration, the base current is obtained from the same equation

$$I_B = \frac{V_{CC}\dfrac{R_{B2}}{R_{B1}+R_{B2}} - V_{BE}}{\dfrac{R_{B1}R_{B2}}{R_{B1}+R_{B2}} + R_E(\beta_F+1)},$$

from where

$$\frac{R_{B2}}{R_{B1}+R_{B2}} = \frac{\dfrac{I_E}{\beta_F+1}\left[\dfrac{R_{B1}R_{B2}}{R_{B1}+R_{B2}} + R_E(\beta_F+1)\right] + V_{BE}}{V_{CC}}. \tag{27}$$

After dividing equation (26) by (27)

$$R_{B1} = \frac{R_E(\beta_F+1)V_{CC}}{mV_{BE} + (m+1)R_E I_E}, \tag{28}$$

where $m \geq 10$ is required for stable biasing. Furthermore, if R_E is known and emitter voltage V_E is chosen by design, the emitter current is

$$I_E = \frac{V_E}{R_E},$$

which enables to define R_{B1} according to the desired emitter bias voltage V_E. Once R_{B1} is known, the other base resistor is evaluated from the equation

$$R_{B2} = \frac{R_E(\beta+1)}{m - \dfrac{R_E}{R_{B1}}(\beta+1)}. \tag{29}$$

To conclude, the bias design procedure could go as follows:

1. select the operating voltage V_{CC}
2. select the emitter bias voltage V_E
3. select R_E to determine emitter current and input/output impedance
4. select the stability multiplier m, which should be larger or equal to 10
5. calculate R_{B1} from equation (28)
6. calculate R_{B2} from equation (29)